Suppression of the Parallel-Plate Noise in High-Speed Circuits Using a Metallic Electromagnetic Band-Gap Structure

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Abstract – **A novel approach for the suppression of the parallel-plate noise in high-speed circuits is proposed by utilizing a metallic electromagnetic band-gap (EBG) structure. The key idea relies on replacing one of the two solid electric conductor plates with a metallic EBG surface of compact texture. To validate the concept, an EBG surface was fabricated and employed in a number of via-containing parallel-plate test boards. Frequency domain measurements showed a band-gap of about 1.7 GHz around 3.77 GHz. More importantly, suppression of the parallel-plate noise by 65% was achieved based on time domain reflectometry experiments.**

I. INTRODUCTION

With the ever-increasing clock frequencies of digital circuits and the emergence of low power integrated circuits, the bottle-neck imposed by the power/ground noise, i.e. the parallel-plate waveguide (PPW) mode referred to as a noise, becomes more and more significant. Therefore, the characterization and suppression of this PPW noise are both deemed crucial in high-speed circuit design. The analysis of this type of noise, excited by vias in a parallel-plate environment has been the focus of many research works [1]. In practice, different techniques are commonly used to suppress the parallel-plate noise which can be summarized as follows:

1) adding discrete decoupling capacitors to provide a grounding path for equalizing the voltage fluctuations on the reference DC voltage planes [2];

2) employing buried decoupling capacitors where parallel planes configure a distributed capacitor. In comparison with discrete capacitors, buried capacitors are less prone to parasitics and have a better performance at higher frequencies [3];

3) selecting the location of the via ports in a manner that eliminates certain package resonances thus leading to the reduction of the coupling between two ports through the parallel-plate noise [4];

4) employing differential interconnect designs which inherently reject the common mode noise [5].

As an alternative to these methods, in the present paper, a metallic electromagnetic band-gap (EBG) structure is proposed to function as a planar band-stop filter that blocks the RF noise currents on power/ground planes. This type of approach for suppressing unwanted RF surface currents has been employed in previous research works such as [6], and [7] but for high-frequency analogue applications. In [6], a uniplanar EBG structure has been utilized to suppress leakage in stripline circuits above 9 GHz. For this purpose, a two-dimensional EBG was realized by etching a periodic slot pattern on both ground planes [6]. Unfortunately, the resulting perforated ground planes are prone to leakage through radiation, especially when operating within the band-gap.

The challenge in employing EBGs for the suppression of the parallel-plate noise in high-speed circuits arises due to two reasons: (a) a typical parallel-plate noise pattern has a low-pass spectrum signature (typically < 6 GHz), thus requiring a compact, low frequency, EBG structure; (b) the EBG band-gap should span enough bandwidth to effectively suppress the PPW noise. A suitable metallic EBG structure that satisfies these requirements and is not prone to radiation leakage seems to be the surface proposed by Sievenpiper et al. for antenna applications [7]. To the best of the authors knowledge, this current paper presents the first application of such an EBG surface for suppressing the parallel-plate noise in high-speed digital circuits. Indeed, this novel approach in suppressing the parallel-plate noise is superior to the other methods mentioned before, because: (i) decoupling capacitors, port allocation methods, or differential interconnects only provide a *localized* suppression of the noise; (ii) all types of decoupling capacitors perform best at their resonance frequency which is unfortunately determined by the parasitics rather than by design parameters. In contrast to the existing methods, the proposed EBG approach provides a *global* solution since it blocks the PPW noise *all over* the EBG ground and *in all azimuthal directions* and can be designed to achieve a specific resonance and band-gap.

The organization of this paper is as follows: First, using a physics-based CAD model for vias in parallel-plate environments [1], the spectrum of the PPW noise in a given

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structure is predicted. Based on this information, an EBG surface is designed to create a relatively wide band-gap at low frequencies. This EBG surface is evaluated through measurements. Finally, time domain reflectometry (TDR) and frequency domain experimental results are presented which demonstrate an efficient suppression/isolation of the parallel-plate noise.

II. DESIGN OF THE EBG STRUCTURE

A single-layer parallel-plate structure, excited by vias is shown in Fig. 1. The physics-based CAD model for vias in parallel-plate environments, developed in [1], is utilized to predict the spectrum of the noise at Port 2 when Port 1 is excited by a 200 mV step voltage with a 110 ps risetime. The spectrum shown in Fig. 2 indicates that the parallel-plate noise has a low-pass signature. If the noise-voltage frequency components that are greater than -65 dB (i.e. -20 dB from the peak level) are defined to be the significant components, a frequency range from 0 to 6 GHz can be identified as the noise bandwidth, as shown in Fig. 2. Hence, a planar low-pass or a band-stop filter with a wide band-gap targeted for this region can efficiently suppress the parallel-plate noise. The compact textured EBG ground-plane proposed in [7], has been selected to realize such a planar omnidirectional band-stop filter. According to [7], as long as the wavelength is much longer than the size of the individual cells, the surface impedance can be represented by an equivalent parallel resonant LC circuit. The relative bandwidth of this LC resonator is proportional to $\sqrt{L/C}$. Therefore, for our intended wide-band application, the ratio of L/C should maintain a relatively large value in the design of the EBG structure. For the total elimination of the parallel plate noise, it is desired to achieve a 6 GHz band-gap, but this proves quite difficult to achieve in practice. Considering the manufacturing constraints and using an iterative design procedure, reasonable values for L and C which simultaneously meet the low frequency but wide-band resonance requirements have been determined to be 2 nH and 1.25 pF, respectively. The resulting resonance frequency for this LC circuit is 3.2 GHz which indeed lies around the center of the noise bandwidth in Fig. 2. In addition this choice leads to a reasonably wide band-gap of 1.7 GHz as will be demonstrated later on.

To maintain a compact design, the three-layer EBG surface of Figure 3 was designed and realized. The corresponding unit cell is the square patch also shown in Fig. 3. Based on the desired resonance frequency and bandwidth, the corresponding physical dimensions of the unit cell, i.e. the size of the patch and height of the via, and the spacing between the cells, have readily been derived using available closed form expressions.

Testing the performance of the EBG structure: The EBG surface of Fig. 3 was fabricated and characterized by the technique suggested in [7], which requires placing two probes at the edges of the surface under test, as presented in the inset diagram of Fig. 4(a). Subsequently, the S21 parameter of the EBG surface is compared with the transmission across a flat metal surface as also shown in Fig. 4(a). It can be seen that the center frequency of the EBG's band-gap is about 3.77 GHz. Moreover, the EBG structure was tested in a parallel-plate environment to investigate any perturbation to the original band-gap. For this purpose, two test structures, each containing two through vias were fabricated. The first test structure was simply the double-sided FR4 board shown in Fig. 1. The second structure was a single-sided FR4 board with the same dimensions as the first board but with the bottom plate now replaced by the EBG surface of Fig. 3. Therefore, the EBG surface of the second test structure, around the resonance frequency, exhibits a very high impedance (open circuit) whereas at lower frequencies behaves like a short circuit, resembling a parallel-plate environment with two electric conductor planes. The insertion loss between Port 1 and Port 2 was measured for both test structures as shown in Fig. 4. It can be observed from Fig 4(b) that the S21 band-gap of the second structure widens (compared to Fig. 3) but still resides around 3.77 GHz. It should be pointed out that from 3.2 GHz to 4.9 GHz, the insertion loss between the two ports in the second (EBG) structure remains higher than 45 dB. In comparison to the S21 of the first test structure (electric conductor grounds), this implies an attenuation of more than 20 dB over a 1.7 GHz band of the noise spectrum.

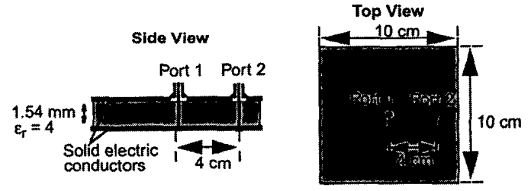

Fig. 1. Single-layer parallel-plate structure.

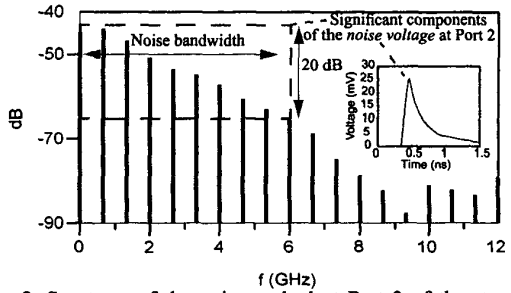

Fig. 2. Spectrum of the noise probed at Port 2 of the structure shown in Fig. 1.

III. IMPROVED PPW NOISE ISOLATION RESULTS

To evaluate the idea of utilizing EBGs to suppress the parallel-plate noise, the test-bed structure shown in Fig. 5, containing one through via and one buried via interconnecting two striplines was fabricated. The stripline-via structure was located closer to the left side of the board and had a 3.5 cm by 10 cm solid conductor ground plane. The rest of the bottom surface, i.e. an area of 6.5 cm by 10 cm, was occupied by the EBG surface of Fig. 3. Finally, a through via was located at the right edge of the EBG ground to monitor the parallel-plate noise. To evaluate the performance of the structure shown in Fig. 5, an identical configuration with a complete (10 cm by 10 cm) conducting bottom ground plane was also fabricated and tested in both time and frequency domains.

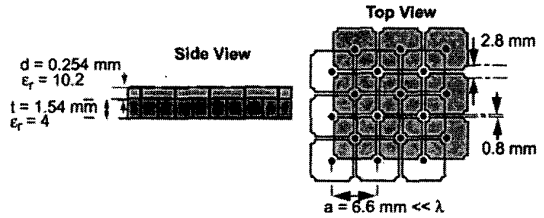

Fig. 3. Diagram of the fabricated EBG surface.

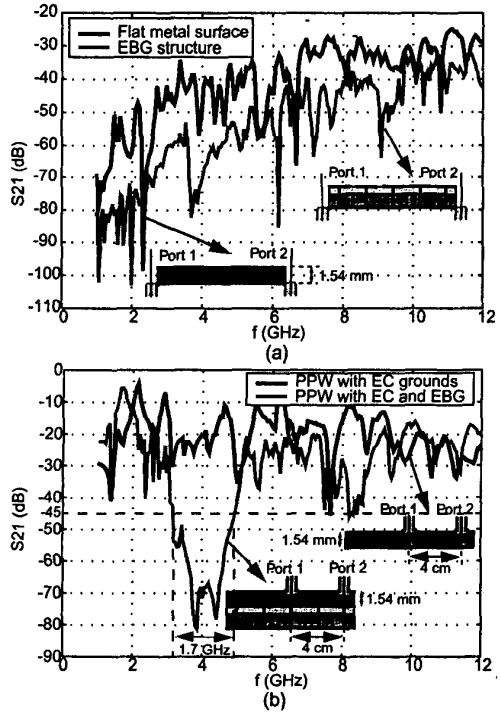

Fig. 4. Measured S21: (a) probes are located at the edges of the EBG surface and a flat metal surface, (b) parallel-plate (PPW) structures with EBG and electric conductor (EC) ground planes.

S-parameter Measurements: The scattering parameters of the three port structure of Fig. 5 were measured and the magnitudes of S21 and S31 are plotted in Fig. 6. In the same figure, the S-parameters of the corresponding structure with two complete grounds are also shown for comparison. It can be seen that the transmission coefficient, S21, of the stripline-via structure next to a partial EBG ground has an identical signature to that of the stripline-via structure with the complete conducting planes. However, the S31 parameter, presented in Fig. 6(b), has a band-gap imposed by the EBG and exhibits an isolation of more than 45 dB over a 1 GHz bandwidth. The same level of isolation exists between Ports 2 and 3. These measurement results corroborate that for the purpose of *isolating* a noisy ground from the rest of the circuit, an efficient solution is to insert an EBG surface in the common ground.

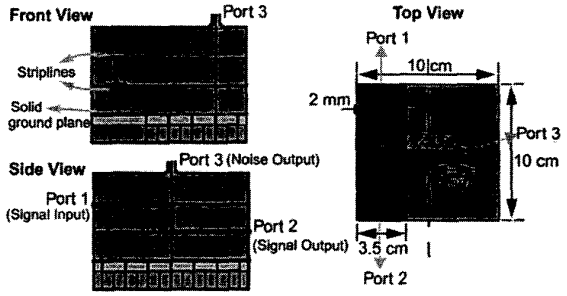

Fig. 5. The stripline-via test-bed structure containing partial electric conductor and EBG planes.

TDR Measurements: Time domain measurements were performed utilizing a TDR set-up that generates a 200 mV step voltage. This signal is launched into the input port (Port 1) of the stripline-via structure shown in Fig. 5. The transmitted signal through the stripline to Port 2 is shown in Fig. 7(a) and has a risetime of 110 ps. As shown, almost identical output waveforms for the two test structures are observed.

The most interesting result is obtained from the measurements of the PPW noise-voltage at Port 3, as presented in Fig. 7(b). It is evident that when the EBG ground is employed, the most prominent feature of the parallel-plate noise, i.e. the noise peak, is reduced by 65%. It is important to point out that this drastic suppression of the parallel-plate noise occurs *all over* the EBG surface and in *all azimuthal directions* as opposed to other, less efficient, localized noise suppression techniques. It should be mentioned that even if the EBG surface replaces the entire bottom ground plane, with a careful choice of the design parameters it is still possible to obtain an almost undistorted transmitted signal on the stripline while achieving an efficient global suppression of the parallel-plate noise.

IV. CONCLUSIONS

A novel approach for the suppression of the parallel-plate noise in high-speed circuits is suggested. Specifically, a metallic EBG surface is proposed to replace one of the electric conductor ground planes in parallel-plate structures containing vias. The EBG structure is realizable at low frequencies (< 6 GHz) leading to compact designs. Since the EBG surface contains no slots, it offers immunity to parasitic radiation and power leakage. Unlike traditional *localized* noise suppression methods, this proposed technique offers the ability to suppress the PPW noise *globally.* To validate the concept, a test-bed structure was fabricated and tested demonstrating a 65% reduction of the PPW noise peak. Additional measurements demonstrated that a bandgap between 1-1.7 GHz (depending on the excitation mechanism) with an insertion loss above 45 dB can be achieved when the EBG structure is inserted in the common ground plane between two ports. Therefore, utilizing EBGs is a convenient technique for enhancing port isolation and segregating noisy grounds.

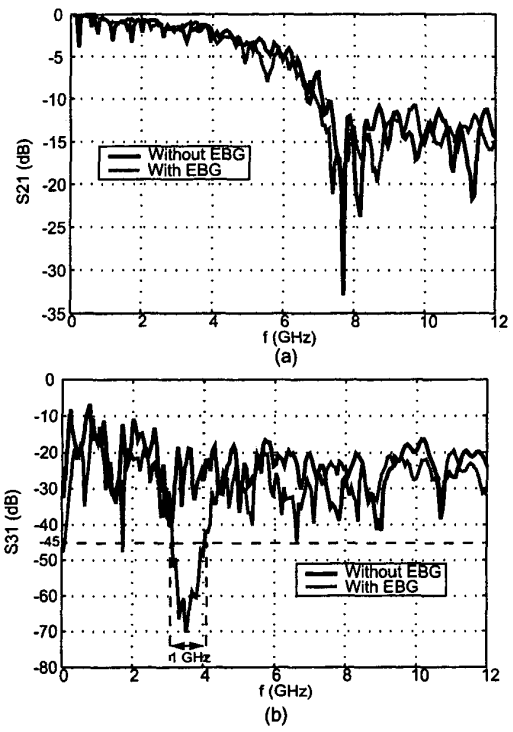

Fig. 6. Measured S-parameters of two stripline-via structures, one is the test-bed of Fig. 5 (With EBG), and the other is the same structure but the bottom surface is a complete electric conductor plane instead (Without EBG). (a) S21, (b) S31.

REFERENCES

[1] R. Abhari, G.V. Eleftheriades and T.E. van Deventer-Perkins, "Physics-based CAD models for analysis of vias in parallel-plate environments," *IEEE Trans. Microwave Theory and Tech.*, Oct. 2001, vol. 49, no. 10, pp. 1697-1707.

[2] M.I. Montrose, *EMC and the printed circuit board design, theory and layout made simple*, IEEE Press, 1999.

[3] Buried Capacitance. [Online]. Available: http://www.merix.com/resourcecntr/tech/bc_dh.doc.

[4] G.-T. Lei, R.W. Techentin, and B. K. Gilbert, "High-frequency characterization of power/ground-plane structures," *IEEE Trans. Microwave Theory and Tech.*, May 1999, vol. 47, no. 5, pp. 562-569.

[5] R. Abhari, G.V. Eleftheriades and T.E. van Deventer-Perkins, "Analysis of differential vias in multilayer parallel plate environment using a physics-based CAD model," *IEEE MTT-S Int. Microwave Symp. Digest*, pp. 2031–2034, May 2001.

[6] K.-P. Ma, J. Kim, F.-R. Yang, Y. Qian, and T. Itoh, "Leakage suppression in stripline circuits using a 2-D photonic bandgap lattice," *IEEE MTT-S Int. Microwave Symp.*, pp.73-76, June 1999.

[7] D. Sievenpiper, L. Zhang, R.F.J. Broas, N.G. Alexopolous, and E. Yablonovitch, "High-Impedance electromagnetic surfaces with a forbidden frequency band," *IEEE Trans. Microwave Theory Tech.*, vol.47, pp. 2059-2074, Nov. 1999.

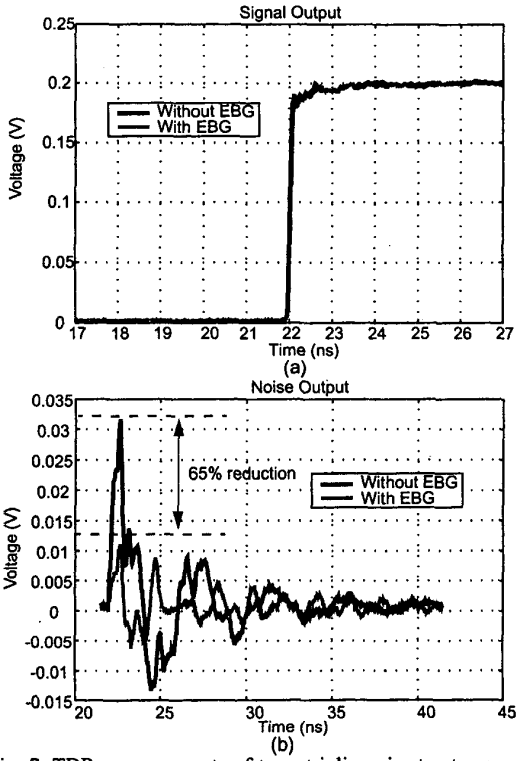

Fig. 7. TDR measurements of two stripline-via structures, one is the test-bed of Fig. 5 (With EBG), and the other is the same structure but the bottom surface is a complete electric conductor plane instead (Without EBG). (a) Output signals at Port 2, (b) Probed noise voltages at Port 3.